Application Note 337
Implementation of ANSI T1.231 On Dallas Semiconductor T1 SCTs

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Overview

The DS2151, DS2152, DS21352, DS21552 and DS2155 single-chip transceivers incorporate all the key performance indications that are required by ANSI T1.231-1997 (originally dated 1993), entitled “Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring.”

Table 1lists all important parameters and where they are located within the DS2151, DS2152, DS21352, DS21552, and DS2155. These T1 transceivers do the raw collection of the data. The devices rely on the external host to accumulate the parameters and create the higher order statistics such as errored seconds, severely errored seconds, LOS seconds, and so on. The one-second timer within these T1 transceivers is ideal for timing these higher order statistics.

Table 1. DS2151 and DS2152 Parameters

PARAMETER	PARAGRAPH	LOCATION WITHIN THE DS2151 AND DS2152
Bipolar Violations (BPV)	6.1.1.1.1	Line Code Violation Count Registers with RCR1.7 = 0
Excessive Zeros (EXZ) (Note 1)	6.1.1.1.2	Line Code Violation Count Registers with RCR1.7 = 1
Cyclic Redundancy Check (CRC)	6.1.1.2.1	Path Code Violation Count Registers
Frame Bit Error (FE) (Note 2)	6.1.1.2.2	1. RIR1.0 2. Path Code Violation Count Registers in D4 framing mode with RCR2.0 = 0 3. Multiframes Out-of-Sync Count Registers in ESF mode with RCR2.0 = 1
Controlled Slip (CS)	6.1.1.2.3	SR1.4 on receive side RIR2.3 on transmit side
Loss of Signal (LOS)	6.1.2.1.1	SR1.1
Out of Frame (OOF)	6.1.2.2.1	SR1.0 (RCR1.4 and RCR1.5 are used to set the criteria.)
Severely Errored Frame (SEF) (Note 3)	6.1.2.2.2	RIR1.2
Alarm Indication Signal (AIS)	6.1.2.2.3	SR1.3

Note 1: The DS2151 and DS2152 only count each excessive zero string once. For example, a string of 48 consecutive zeros would only increment the line code violation count registers once, not multiple times.

Note 2: Via the RCR2.1 bit, the user has the choice in the D4 framing mode of counting errors in just the Ft-bit pattern or in both the Ft-bit and the Fs-bit patterns.

Note 3: In the D4 framing mode, the SEFE bit (RIR1.2) only counts errors in the Ft-bit pattern; in the ESF framing mode, only errors in the FPS pattern are counted.

Table 2. DS21352 and DS21552 Parameters

PARAMETER	PARAGRAPH	LOCATION WITHIN THE DS21352 AND DS21552
Bipolar Violations (BPV) (Note 1)	6.1.1.1.1	Line Code Violation Count Registers with RCR1.7 = 0
Excessive Zeros (EXZ) (Note 1)	6.1.1.1.2	Line Code Violation Count Registers with RCR1.7 = 1
Cyclic Redundancy Check (CRC)	6.1.1.2.1	Path Code Violation Count Registers (Upper nibble of the PCVCR1 register is used for MOSCR1)
Frame Bit Error (FE) (Note 2)	6.1.1.2.2	1. RIR1.0 2. Path Code Violation Count Registers in D4 framing mode with RCR2.0 = 0 3. Multiframes Out-of-Sync Count Registers in ESF mode with RCR2.0 = 1
Controlled Slip (CS)	6.1.1.2.3	SR1.4 on receive side RIR2.3 on transmit side
Loss of Signal (LOS)	6.1.2.1.1	SR1.1
Out of Frame (OOF)	6.1.2.2.1	SR1.0 (RCR1.4 and RCR1.5 are used to set the criteria)
Severely Errored Frame (SEF) (Note 3)	6.1.2.2.2	RIR1.2
Alarm Indication Signal (AIS)	6.1.2.2.3	SR1.3

Note 1: Table 3 shows the counting arrangements for the Line Code Violation Count Registers on the DS21352 and the DS21552.
Note 2: Via the RCR2.1 bit, the user has the choice in the D4 framing mode of counting errors in just the Ft bit pattern or in both the Ft and the Fs bit patterns.
Note 3: In the D4 framing mode, the SEFE bit (RIR1.2) only counts errors in the Ft pattern; in the ESF framing mode, only errors in the FPS pattern are counted.

Table 3. Counting Arrangements for Line Code Violation Registers

COUNT EXCESSIVE ZEROS (RCR1.7)	B8ZS ENABLED (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs
No	No	BPV
Yes	No	BPVs + 16 Consecutive Zeros
No	Yes	BPVs (B8ZS Codewords Not Counted)
Yes	Yes	BPV's + 8 Consecutive Zeros

Table 4. DS2155 Parameters

PARAMETER	PARAGRAPH	LOCATION WITHIN THE DS2155
Bipolar Violations (BPV) (Note 1)	6.1.1.1.1	Line Code Violation Count Registers with ERCNT.0 = 0
Excessive Zeros (EXZ) (Note 1)	6.1.1.1.2	Line Code Violation Count Registers with ERCNT.0 = 1
Cyclic Redundancy Check (CRC) (Note 2)	6.1.1.2.1	Path Code Violation Count Registers (PCVCRF bit is used with MOSCRF bit)
Frame Bit Error (FE) (Note 3)	6.1.1.2.2	1. INFO1.0 2. Path Code Violation Count Registers in D4 framing mode with ERCNT.1 = 0 3. Multiframes Out-of-Sync Count Registers in ESF mode with ERCNT.1 = 1
Controlled Slip (CS)	6.1.1.2.3	SR5.0 on receive side SR5.3 on transmit side
Loss of Signal (LOS)	6.1.2.1.1	SR2.0
Out of Frame (OOF) (Note 4)	6.1.2.2.1	SR1.3 (T1RCR1.4 (OOF2) and T1RCR1.5 (OOF1) are used to set the criteria)
Severely Errored Frame (SEF) (Note 5)	6.1.2.2.2	INFO1.2
Alarm Indication Signal (AIS)	6.1.2.2.3	SR2.2

Note 1: Table 5 shows the the counting arrangements for the Line Code Violation Count Registers on the DS2155.
Note 2: Table 6 shows the detailed description of exactly what errors the PCVCR counts on the DS2155.
Note 3: Via the ERCNT.2 bit, the user has the choice in the D4 framing mode of counting errors in just the Ft bit pattern or in both the Ft and the Fs bit patterns.
Note 4: Table 7 contains the out-of-frame selection criteria.
Note 5: In the D4 framing mode, the SEFE bit (INFO1.2) only counts errors in the Ft pattern; in the ESF framing mode, only errors in the FPS pattern are counted.

Table 5. LCVCR Register in DS2155

COUNT EXCESSIVE ZEROS (ERCNT.0)	B8ZS ENABLED (T1RCR2.5)	WHAT IS COUNTED IN THE LCVCRs
No	No	BPV
Yes	No	BPVs + 16 Consecutive Zeros
No	Yes	BPVs (B8ZS Codewords Not Counted)
Yes	Yes	BPV’s + 8 Consecutive Zeros

Table 6. T1 Path Code Violation Counting Arrangements Using PCVCR Register in DS2155

FRAMING MODE	COUNT Fs ERRORS?	WHAT IS COUNTED IN THE PCVCRs
D4	No	Errors in the Ft Pattern
D4	Yes	Errors in Both the Ft and Fs Patterns
ESF	Don't Care	Errors in the CRC6 Codewords

Table 7. Out-of-Frame Criteria Selection in DS2155

OOF2	OOF1	OUT-OF-FRAME CRITERIA
0	0	2/4 Frame Bits in Error
0	1	2/5 Frame Bits in Error
1	0	2/6 Frame Bits in Error
1	1	2/6 Frame Bits in Error